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In the United States Patent and Trademark Office

Date:	May 4, 2005		
In re Application of:	Austin, et al.	*Filed:*	05/28/2004
For:	Programmable Frequency Divider with Symmetrical Output		
Serial Number:	10/709,804	*Confirmation Number:*	3803
Art Unit:	2816	*Examiner:*	Wambach, Margaret R.

REPLY AND AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner of Patents & Trademarks
Alexandria, VA 22313

Sir:

This is in response to the Office Action mailed on February 4, 2005, which is due for response by May 4, 2005. Any fees required in entering this response may be charged to Applicant's deposit account, 09-0456.

It is respectfully requested that this Amendment be entered in the above referenced application and reconsideration of the application in view of these comments be made. No new matter has been included. The application should be amended as follows:

In the Specification

Amend the following numbered paragraphs of the specification:

[0005] The performance requirements of divider circuits have increasingly demanded a greater number of divide modes, a wider divide range, and the smallest possible divide resolution. There are currently many divider styles in use that address each of these requirements individually. The real challenge, however, is to meet ~~these~~ all of these requirements along with the additional demands that a divider circuit be able to process higher signal frequencies, occupy less physical area and consume less power.

[0032] Fig. 17 depicts a frequency divider circuit wherein the symmetrical divider of Fig. 16 is replaced with a symmetrical divide-by-four component.

[0039] Fig. 24 ~~depicts the state transition table for LFSR of Fig. 23~~ shows an eight latch LFSR with a multistage XOR feedback network distributed across multiple latches.

[0040] Fig. 25 ~~shows an eight latch LFSR with a multistage XOR feedback network distributed across multiple latches~~ depicts the state transition table for LFSR of Figs. 23 and 24.

[0086] Because the logical XOR is distributed across two clock cycles, it is possible that the latch L0 will not reflect the value it would have had in the original single cycle feedback network of Fig. 23. With the modified feedback structure, latch L0 will now occasionally contain a known "false" value that will be corrected during the next clock cycle via the XOR 204 between latches L0 and L1 in Fig. ~~25~~ 24. The table 206 in Fig. 26 illustrates the progression of several LFSR states. These same states are listed in the table of Fig. ~~24~~ 25.

[0096] A fifth embodiment of the high speed LFSR counter of the frequency divider, shown in Fig. 34, adds an additional programmability feature by providing a multiplexed input to each of the LFSR latches. The LFSR counter latches can be initialized to specific values via a latch RESET

input. Another latch 250 is added to control the gates of the ~~multiplexor~~ multiplexer circuits used for programming the maximum state count.

In the Claims

Amend claims 1-25 as follows:

1.(Original) A high speed programmable divider circuit with symmetrical duty cycle, comprising:

a division mode controller capable of specifying a binary encoded divisor value;

a linear feedback shift register (LFSR) coupled to the division mode controller and forming a first stage divide function;

a master-slave latch coupled in series with the LFSR and forming a second stage divide function;

a duty cycle correction circuit coupled in series with the master-slave latch; and

an inverter with an input coupled to a slave output of the master-slave latch and to the duty cycle correction circuit and an output coupled to the division mode controller and the data input of the master-slave latch.

2. (Original) The high speed programmable divider circuit according to claim 1, wherein the division mode controller is adapted to alternate the divisor value every clock cycle by one more or one less than a desired final divisor value for an odd numbered final divisor value.

3. (Currently Amended) The high speed programmable divider circuit according to claim 1, further comprising:

a logic gate coupled to the LFSR output and driving the second stage divide~~r element~~ function; and

a latch controlling a final divide value of the division mode controller.

4. (Original) The high speed programmable divider circuit according to claim 1, wherein the LFSR comprises:

a plurality of series coupled latch elements forming a counter capable of producing an odd number of counter states;

a pipeline latch element coupled in parallel with one of the plurality of latch elements;

a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and

an output logic element coupled to the outputs of each of the plurality of latch elements of the counter, the output logic element capable of detecting a complete cycle of the counter states.

5. (Currently Amended) The high speed programmable divider circuit according to claim 3, wherein the second stage divide ~~element~~ function comprises a divide-by-two latch.

6. (Currently Amended) The high speed programmable divider circuit according to claim 3, wherein the second stage divide ~~element~~ function comprises a divide-by-four latch pair.

7. (Currently Amended) The high speed programmable divider circuit according to claim 3, wherein the second stage divide ~~element~~ function comprises a plurality of m latches, where m is an even integer.

8. (Currently Amended) The high speed programmable divider circuit according to claim 7, wherein the second ~~divider~~ stage divide function includes a plurality of ~~multiplexor~~ multiplexer elements to control phase alignment of ~~the~~ an output of the ~~frequency~~ divider circuit.

9. (Currently Amended) The high speed programmable divider circuit according to claim 8, further comprising:

a second divider circuit coupled in parallel with the high speed programmable ~~frequency~~ divider circuit and forming a multiple divider; and

a synchronization circuit coupled to the multiple divider capable of detecting synchronization of output transitions from the multiple divider and generating a synchronization signal.

10. (Currently Amended) The high speed programmable divider circuit of claim 9, wherein the second divider specifies a final divisor that is different from the divisor of the ~~frequency~~ divider circuit.

11. (Currently Amended) A method of performing a frequency division of a digital waveform, the method comprising:

specifying a binary encoded divisor using a division mode controller;

forming a first stage divide function using a linear feedback shift register (LFSR) coupled to the division mode controller ~~and~~;

forming a second stage divide function using a master-slave latch coupled in series with the LFSR ~~and~~;

generating a symmetrical ~~output of the~~ frequency division output using a duty cycle correction circuit coupled in series with the ~~master/slave~~ master-slave latch;

selecting a divisor value of the LFSR as a function of a desired final divisor value to perform an even or an odd divide-by function;

alternating the divisor value of the LFSR by one more or one less than the desired final divisor value for an odd numbered final divisor value; and

maintaining the divisor value of the LFSR for an even numbered final divisor value.

12. (Original) The method according to claim 11 further comprising:

changing the final divisor value synchronously with an output pulse of the LFSR.

13. (Currently Amended) The method according to claim 11, further comprising:

forming a multiple divider circuit by operating a second frequency divider in parallel with a first frequency divider;

synchronizing ~~the~~ a first output and a second outputs of the multiple divider; and

maintaining a specified phase relationship between the outputs of the first frequency divider and the second frequency divider.

14. (Currently Amended) A high speed linear feedback shift register (LFSR), comprising:

a plurality of series coupled latch elements forming a counter capable of producing an odd number of counter states;

a pipeline latch element coupled in parallel with one of the plurality of latch elements;

a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and

an output logic element coupled to ~~the~~ an outputs of each of the plurality of latch elements of the counter, the output logic element capable of detecting a complete cycle of ~~the~~ counter states.

15. (Original) A high speed linear feedback shift register (LFSR), comprising:

a first plurality of series coupled latch elements forming a first counter capable of producing an odd number of counter states;

a second plurality of series coupled latch elements coupled in parallel with the first plurality of latch elements, the second plurality of latch elements forming a second counter capable of producing an even number of counter states;

a feedback logic network decomposed into multiple logic stages and distributed across multiple latch elements of the first counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay, the feedback logic network adapted to generate a primitive polynomial; and

an output logic element coupled to the outputs of each of the plurality of latch elements of the first counter and the second counter, the output logic element capable of detecting a complete cycle of the LFSR counter states.

16. (Original) The high speed LFSR according to claim 15, wherein the second counter element comprises a divide-by-two latch.

17. (Currently Amended) The high speed LFSR according to claim 15, wherein the second counter ~~element~~ comprises a divide-by-four latch pair.

18. (Currently Amended) The high speed LFSR according to claim 15, wherein the second counter ~~element~~ comprises a divide-by-n latch, where n is an even integer.

19. (Currently Amended) The high speed LFSR ~~programmable divider circuit~~ according to claim 15, wherein the feedback logic network comprises an XOR gate coupled to an output of a first LFSR latch and to the output of a second LFSR latch and to the input of a third LFSR latch.

20. (Original) The high speed LFSR according to claim 19, wherein the logic function of the XOR gate is decomposed into multiple logic stages and distributed across multiple latch elements of the first counter such that a maximum latch-to-latch operational latency of the LFSR does not exceed one gate delay.

21. (Currently Amended) The high speed LFSR according to claim ~~14~~ 15, wherein the feedback logic network comprises:

a network of XOR gates distributed across multiple latch elements of the first counter such that a maximum latch-to-latch operational latency does not exceed one XOR gate delay; and

a first pipeline latch element accepting an output from a first XOR gate, the pipeline latch element being coupled in parallel with one of the first plurality of latch elements.

22. (Original) A high speed linear feedback shift register, comprising:

a plurality of series coupled latch elements forming a first counter capable of producing an odd number of counter states;

a second counter coupled in parallel with the first counter, the second counter capable of producing an even number of counter states;

a multi-stage feedback logic network distributed across the plurality of latch elements of the first counter such that the maximum latch-to-latch operational latency of the first counter does not exceed one gate delay;

a first pipeline latch capable of storing a first parallel output of a first stage of the feedback logic network, the first pipeline latch coupled in parallel with one of the plurality of latch elements of the first counter; and

an output logic element coupled to ~~the~~ an outputs of each of the plurality of latch elements of the first counter, the output logic element adapted to detect a unique counter state of the LFSR.

23. (Currently Amended) The high speed LFSR according to claim 22, wherein the multistage feedback network includes a ~~second~~ logic stage coupled between a first latch element and a second latch element of the plurality of latch elements of the first counter.

24. (Currently Amended) The high speed LFSR according to claim 22, further comprising:

a plurality of ~~multiplexor~~ multiplexer elements corresponding to each of the plurality of latch elements of the first counter, the ~~multiplexor~~ multiplexer elements providing a programming function of the LFSR;

a latch element controlling the ~~multiplexor~~ multiplexer elements; and

a reset latch coupled to the output logic element.

25. (Currently Amended) A method of forming a high speed LFSR, the method comprising:

forming a first counter capable of producing an odd number of counter states using a first plurality of series coupled latch elements;

forming a second counter capable of producing an even number of counter states using a second plurality of series coupled latch elements coupled in parallel with the first plurality of latch elements;

generating a primitive polynomial using a feedback logic network decomposed into multiple logic stages;

distributing a feedback logic network across multiple latch elements of the first counter such that a latch-to-latch operational latency of the LFSR does not exceed one gate delay;

storing a first parallel output of a first stage of the feedback logic network in a first pipeline latch coupled in parallel with one of the plurality of latch elements of the first counter; and

detecting a complete cycle of the ~~LFSR~~ counter states using an output logic element coupled to the outputs of each of the plurality of latch elements of the first counter and the second counter.

Remarks

Claims 1-25 are pending in the application. Claims 3, 5-14 and 17-25 stand rejected but contain allowable subject matter, claims 11 and 22-24 are objected to but contain allowable subject matter and claims 1, 2, 4, 15 and 16 have been allowed. By this amendment claims 3, 4-11, 13, 14, 17-19, 21, 23-25 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

The Examiner objected to the disclosure, stating that the pages of the specification should be numbered. Applicants respectfully submit that the application as prepared and submitted for electronic filing using ABX and ePave software should contain page numbers in the upper right hand corner of the document. Applicants will provide a substitute specification upon request by the Examiner.

Claim Objections

The Examiner objected to claims 11 and 22-24 due to a number of informalities. Claims 11 and 22 now recite "(LFSR)" following the first mention of a "linear feedback shift register" to provide a more direct antecedent for later references of the term. Claim 11 has also been amended to make terminology referring to the master-slave latch consistent. Claim 23 has been amended to delete the reference to a "second" logic stage. Finally, the spelling of "multiplexer" has been corrected in Claim 24.

Claim Rejections - 35 U.S.C. § 112

The Examiner rejected claims 3, 5-10, 14 and 17 through 25 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner indicated that the last two lines of claim 10 were indecipherable and

therefore fail to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicants have amended claim 10 in accordance with the Examiner's suggested changes and respectfully submit that claim 10 is condition for allowance.

The Examiner identified a number of recited elements in claims 3, 8, 9, 11, 13, 14, 17-22 and 25 lacking a direct antecedent basis. Accordingly, Applicants have amended claims 3, 8, 9, 11, 13, 14, 17-22 and 25 to correct the cited defects and respectfully submit that the rejection under 35 U.S.C. § 112, second paragraph has been overcome and that all claims are in condition for allowance.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 3, 5-10, 12, 13, 17-21, 23 and 24, stating that such claims would be allowable if amended to overcome the rejection under 35 U.S.C. § 112, second paragraph.

Applicants further acknowledge the Examiner's indication of allowable subject matter in claims 11, 14, 22 and 25, stating that such claims would be allowable if amended to overcome the rejection under 35 U.S.C. § 112, second paragraph.

Applicants respectfully submit that claims 3, 5-11, 13, 14 and 17-25 have been amended to overcome the Examiner's rejection under 35 U.S.C. § 112, second paragraph and are therefore in condition for allowance.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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